ELECTRONIC DOOR LOCK SYSTEM FINAL PRESENTATION

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TEAM 5

강민우 201211324
임동현 201211353
Presenter → 서동현 201211375
함진아 201211389

Contents

PART 1
PURPOSE

PART 1 PURPOSE

UTR FEEDBACK

- Unit Test의 목적을 제대로 숙지하여 설계 상의 문제점을 찾아내어 수정한다.
- 결과로 나온 Fail이 현재 프로그램에서 발생할 확률이 거의 없는 상황이라도, 모듈의 정확성이 떨어지므로 설계 수정 !

FINAL END

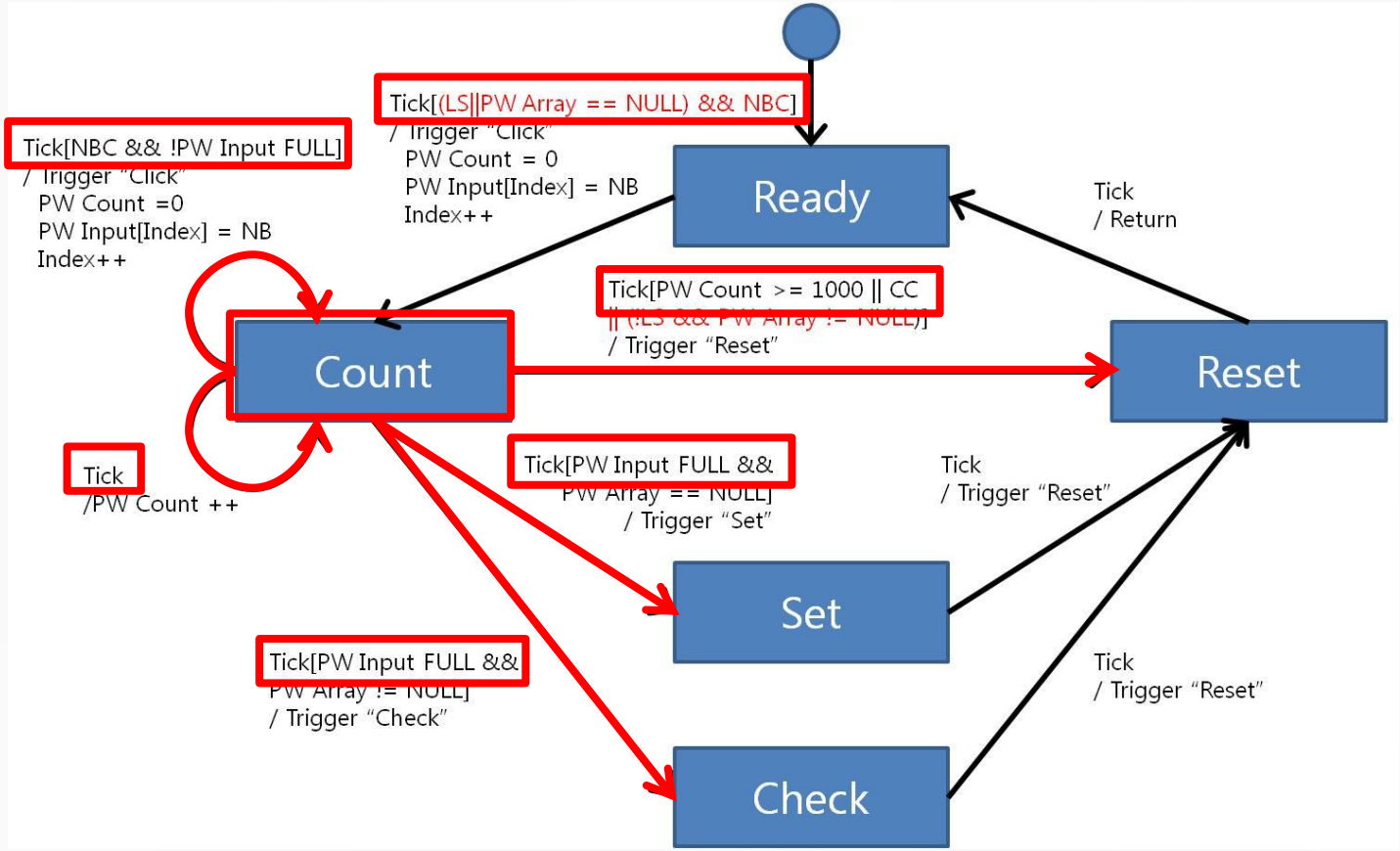
- EDLS 프로그램 최종 결과 산출
- 전체 과정 Summary

PART 2
PROBLEM IN UTR

PART 2 PROBLEM IN UTR

STD CONDITION

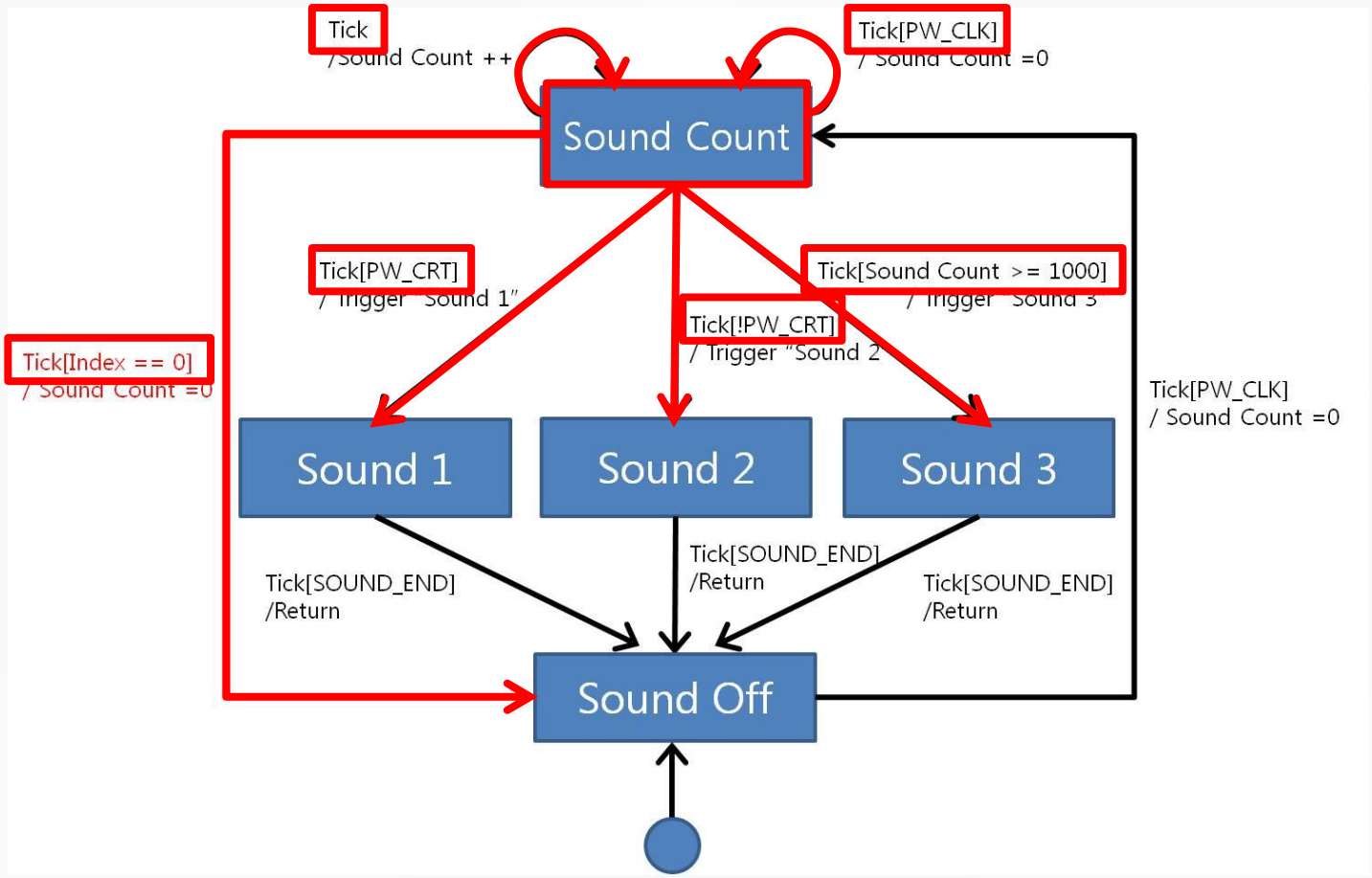
●Index 조건 !



PART 2 PROBLEM IN UTR

STD CONDITION

●Index 조건 !



PART 2 PROBLEM IN UTR

CARELESS

- 발생한 fail을 단순히 Unit Test Case의 문제로 치부

  → 확장 가능성을 고려하지 않은 경솔함 !

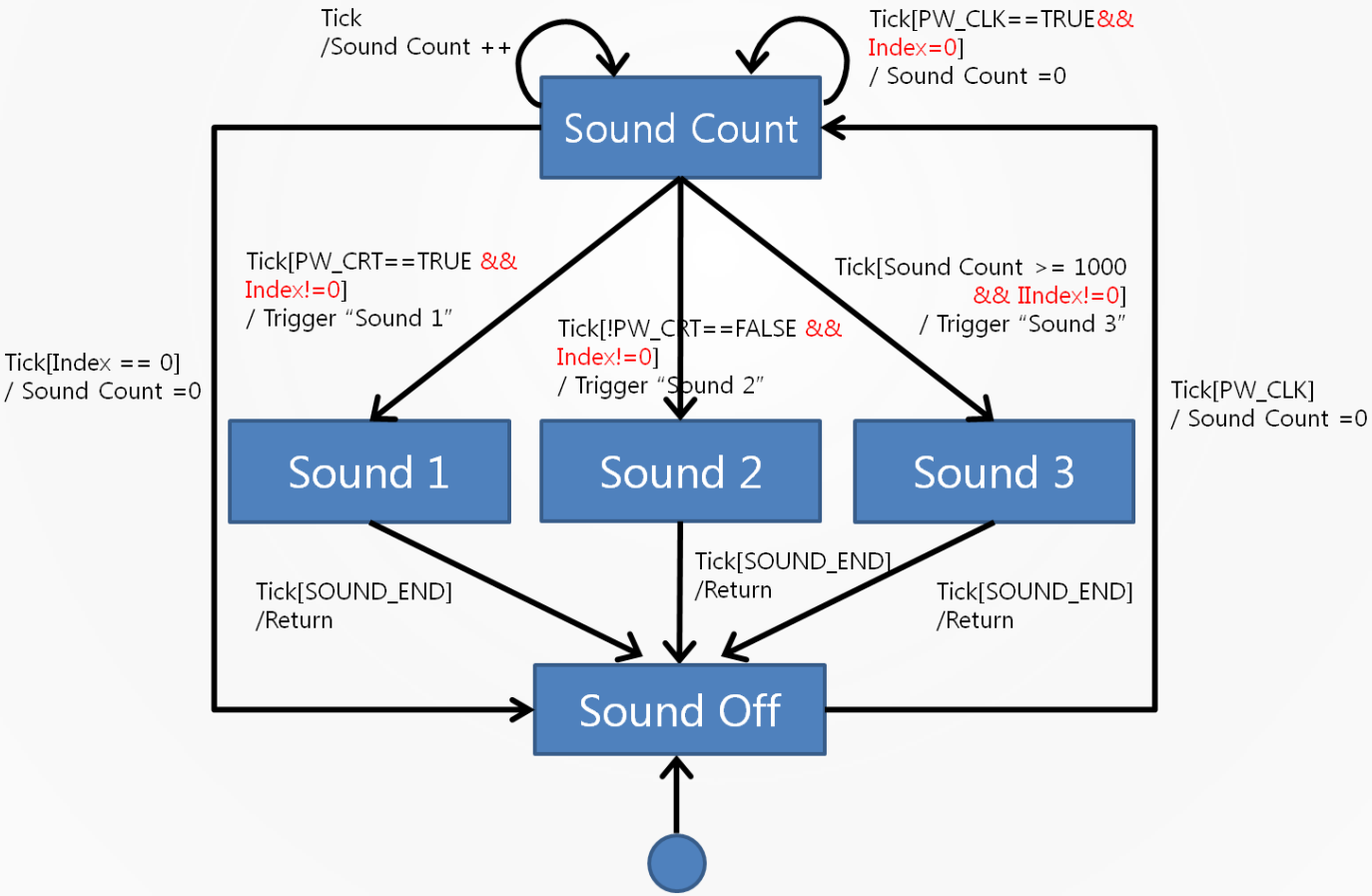
FAIL

```
   src_file:line# : (suite:test) : failure_condition

1. ..\src\cunittest.c:2152 : (1.6. Determine Signal : EDLS_UTC_160_005) : CU_ASSERT_EQUAL(bss_data->numbtn_data->num_button,-1)
2. ..\src\cunittest.c:2229 : (1.6. Determine Signal : EDLS_UTC_160_012) : CU_ASSERT_EQUAL(bss_data->numbtn_data->num_button,-1)
3. ..\src\cunittest.c:2240 : (1.6. Determine Signal : EDLS_UTC_160_013) : CU_ASSERT_EQUAL(bss_data->numbtn_data->num_button,-1)
4. ..\src\cunittest.c:2273 : (1.6. Determine Signal : EDLS_UTC_160_016) : CU_ASSERT_EQUAL(bss_data->numbtn_data->num_button,-1)
5. ..\src\cunittest.c:2284 : (1.6. Determine Signal : EDLS_UTC_160_017) : CU_ASSERT_EQUAL(bss_data->numbtn_data->num_button,-1)
6. ..\src\cunittest.c:2295 : (1.6. Determine Signal : EDLS_UTC_160_018) : CU_ASSERT_EQUAL(bss_data->numbtn_data->num_button,-1)
7. ..\src\cunittest.c:339 : (2.1.1 PW_Controller : EDLS_UTC_211_010) : pw_state == COUNT
8. ..\src\cunittest.c:1580 : (2.2.1 Sound_Controller : EDLS_UTC_221_004) : state==Sound_Count_Mod
9. ..\src\cunittest.c:1652 : (2.2.1 Sound_Controller : EDLS_UTC_221_008) : state==Sound_Count_Mod

--------------------------------------------------------
Total Number of Failures : 9
```

PART 3
MODIFICATION

PART 3 MODIFICATION

SOUND CONTROLLER



PART 3 MODIFICATION

SOUND CONTROLLER

EDLS_UTC_221_000 `	State==Sound Off / PW_CLK==TRUE	State==Sounds Count / Sound_Count==0
EDLS_UTC_221_001	State==Sound Off/ PW_CLK==False	State==Sound Off
EDLS_UTC_221_002	State==Sound Off / PW_CRT==TRUE	State==Sound Off
EDLS_UTC_221_003	State==Sounds Count / PW_CLK==TRUE, Index==1	State==Sounds Count / Sound_Count==0
EDLS_UTC_221_004	State==Sounds Count/PW_CLK==FALSE	State==Sounds Count
EDLS_UTC_221_005	State==Sounds Count / PW_CRT==TRUE, Index==1	State==Sound 1 / Trigger "Sound 1"
EDLS_UTC_221_006	State==Sounds Count / PW_CRT==FALSE, Index==1	State==Sound 2 / Trigger "Sound 2"
EDLS_UTC_221_007	State==Sounds Count / Sound_Count>=1000, Index==1	State==Sound 3 / Trigger "Sound 3"
EDLS_UTC_221_008	State==Sounds Count / Sound_Count<1000	State==Sounds Count
EDLS_UTC_221_009	State==Sounds Count / Sound_Count<1000, Tick	State==Sounds Count / Sound_Count++
EDLS_UTC_221_010	State==Sounds Count/ Index==0	State==Sound Off
EDLS_UTC_221_011	State==Sounds Count/ Index!=0	State==Sounds Count

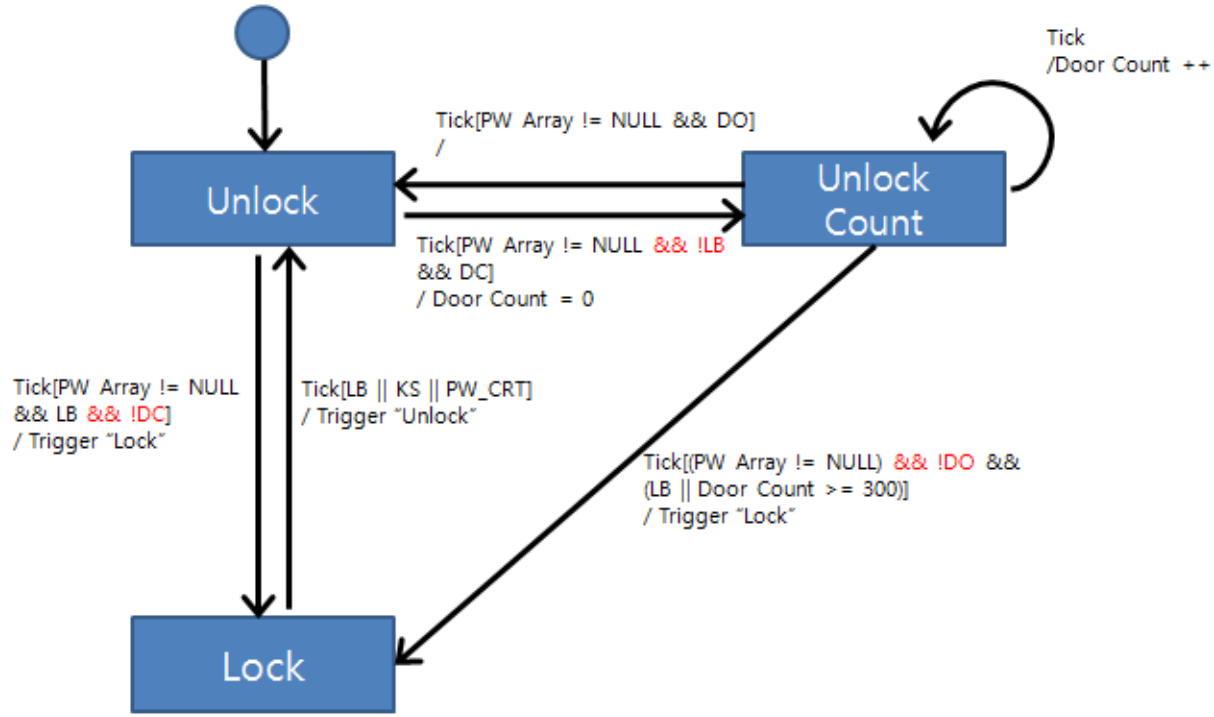
PART 3 MODIFICATION

SOUND CONTROLLER

```
if(pw_crt==TRUE && index != 0){
    *state = Sound_1;    //상태변화
    //        *Sound_Command=Sound1();   //Trigger 'Sound1'
    return Sound1();
}
else if(pw_crt==FALSE && index != 0){
    *state = Sound_2;    //상태변화
    //        *Sound_Command=Sound2();   //Trigger 'Sound2'
    return Sound2();
}
else if(*Sound_Count >= 1000 && index != 0){
    *state = Sound_3;    //상태변화
    //        *Sound_Command=Sound3();   //Trigger 'Sound3'
    return Sound3();
}
else if(pw_clk==TRUE && index != 0)
    *Sound_Count = 0;  //Sound Count 초기화
```

PART 3 MODIFICATION

LOCK CONTROLLER



EDLS_UTC_216_000	State==Unlock/PW Array!=Null, LB==True ,DC==True	State=Unlock
EDLS_UTC_216_001	State==Unlock/PW Array!=Null, LB==False ,DC==True	State=Unlock Count , DoorCount=0
EDLS_UTC_216_002	State==Unlock/PW Array!=Null, LB==True ,DC==False	State=Lock , Trigger'Lock'
EDLS_UTC_216_003	State==Unlock/PW Array!=Null, LB==False ,DC==False	State=Unlock

PART 3 MODIFICATION

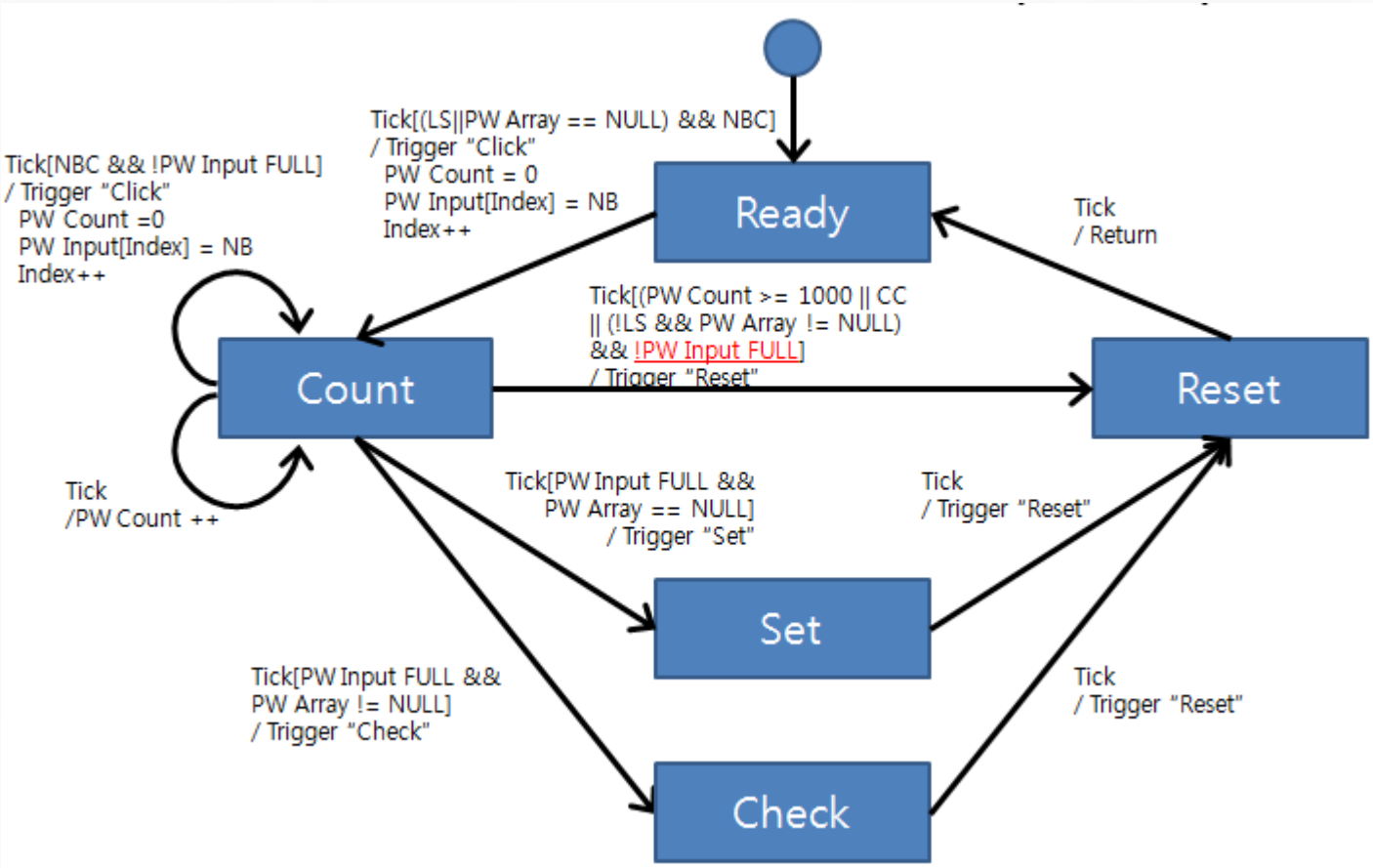
LOCK & LIGHT CONTROLLER

```
case Unlock:
    //문이 닫혔을 경우
    if (pwd->arr != NULL && (LB == FALSE) && (sens_data->dac_data.door_closed_data == TRUE)) {
        *Door_Count = 0;
        *State = Unlock_Counts;
    }
    //lock button이 눌린 경우
    else if (pwd->arr != NULL && (LB == TRUE) && !(sens_data->dac_data.door_closed_data == TRUE)) {
        *State = Lock;
        LockP(cmd);
    }
    break;
    //잠금상태
```

```
case Unlock_Counts:
    //비밀번호 설정된 상태에서 문 열림
    if (pwd->arr != NULL && (sens_data->dac_data.door_opened_data == TRUE)) {
        *State = Unlock;
        //UnlockP(cmd);
        //비밀번호 설정된 상태에서 락버튼 눌리거나 3초이상 시간이 지남
    } else if (pwd->arr != NULL && !(sens_data->dac_data.door_opened_data == TRUE) && ((LB == TRUE) || (*Door_Count >= 300))) {
        *State = Lock;
        LockP(cmd);
    } else{
        (*Door_Count)++;
    }
    break;
```

PART 3 MODIFICATION

PW CONTROLLER



PART 3 MODIFICATION

PW CONTROLLER

	/Index!=4.,	
EDLS_UTC_211_018.,	State==Count / PW Count>=1000 / CC==FALSE, LS==TRUE, PW Array!=NULL /Index!=4.,	State==Reset / Trigger "Reset" .,
EDLS_UTC_211_019.,	State==Count / PW Count>=1000 / CC==FALSE, LS==TRUE, PW Array==NULL /Index!=4.,	State==Reset / Trigger "Reset" .,
EDLS_UTC_211_020.,	State==Count / PW Count>=1000 / CC==FALSE, LS==FALSE, PW Array!=NULL /Index!=4.,	State==Reset / Trigger "Reset" .,
EDLS_UTC_211_021.,	State==Count / PW Count>=1000 / CC==FALSE, LS==FALSE, PW Array==NULL /Index!=4.,	State==Reset / Trigger "Reset" .,
EDLS_UTC_211_022.,	State==Count / PW Count<1000 / CC==TRUE, LS==TRUE, PW Array!=NULL /Index!=4.,	State==Reset / Trigger "Reset" .,
EDLS_UTC_211_023.,	State==Count / PW Count<1000 / CC==TRUE, LS==TRUE, PW Array==NULL /Index!=4.,	State==Reset / Trigger "Reset" .,
EDLS_UTC_211_024.,	State==Count / PW Count<1000 / CC==TRUE, LS==FALSE, PW Array!=NULL /Index!=4.,	State==Reset / Trigger "Reset" .,
EDLS_UTC_211_025.,	State==Count / PW Count<1000 / CC==TRUE, LS==FALSE, PW Array==NULL /Index!=4.,	State==Reset / Trigger "Reset" .,
EDLS_UTC_211_026.,	State==Count / PW Count<1000 / CC==FALSE, LS==TRUE, PW Array!=NULL /Index!=4.,	State==Count .,
EDLS_UTC_211_027.,	State==Count / PW Count<1000 / CC==FALSE, LS==TRUE, PW Array==NULL /Index!=4.,	State==Count .,
EDLS_UTC_211_028.,	State==Count / PW Count<1000 / CC==FALSE, LS==FALSE, PW Array!=NULL .,	State==Reset / Trigger "Reset" .,
EDLS_UTC_211_029.,	State==Count / PW Count<1000 / CC==FALSE,	State==Count .,

PART 3 MODIFICATION

PW CONTROLLER

```
case COUNT:
    (*pw_count)++;                  //Tick 조건 : 무조건 증가
    if(nbd->num_ck && pwd->index != PW_SIZE          //Count 조건
    {
        *pw_clk = pw_click(&nbd->num_ck);      //pw_clk 값 반환받아오기(Trigger)
        *pw_count = 0;                  //pw_count값 초기화
        pwd->input[pwd->index] = nbd->num_button;    //input에 nb 삽입
        (pwd->index)++;                 //index 증가
        nbd->num_button = NIL;                  //nb값 초기화(nbc는 pw_click에서 초기화 됨)
    }
    else if((*pw_count >= 1000 || CC || (!ls && pwd->arr != NULL))&&pwd->index != PW_SIZE
    {
        pw_reset(&pwd->index);
        *pw_state = RESET;
    }
    else if(pwd->index == PW_SIZE && pwd->arr == NULL)
    {
        pw_set(pwd);
        *pw_state = SET;
    }
    else if(pwd->index == PW_SIZE && pwd->arr != NULL)
    {
        *pw_crt = pw_check(pwd);
        *pw_state = CHECK;
    }
    break;
```

PART 4
FINAL RESULT

PART 4 FINAL RESULT

DETERMINE SIGNAL

CUnit - A Unit testing framework for C.
http://cunit.sourceforge.net/

Running Suite 1.6. Determine Signal

Running test EDLS_UTC_160_000 ...	Passed
Running test EDLS_UTC_160_001 ...	Passed
Running test EDLS_UTC_160_002 ...	Passed
Running test EDLS_UTC_160_003 ...	Passed
Running test EDLS_UTC_160_004 ...	Passed
Running test EDLS_UTC_160_005 ...	Passed
Running test EDLS_UTC_160_006 ...	Passed
Running test EDLS_UTC_160_007 ...	Passed
Running test EDLS_UTC_160_008 ...	Passed
Running test EDLS_UTC_160_009 ...	Passed
Running test EDLS_UTC_160_010 ...	Passed
Running test EDLS_UTC_160_011 ...	Passed
Running test EDLS_UTC_160_012 ...	Passed
Running test EDLS_UTC_160_013 ...	Passed
Running test EDLS_UTC_160_014 ...	Passed
Running test EDLS_UTC_160_015 ...	Passed
Running test EDLS_UTC_160_016 ...	Passed
Running test EDLS_UTC_160_017 ...	Passed
Running test EDLS_UTC_160_018 ...	Passed

PART 4 FINAL RESULT

PW CONTROLLER

Running Suite 2.1.1 PW_Controller

Running test EDLS_UTC_211_000 ...	Passed
Running test EDLS_UTC_211_001 ...	Passed
Running test EDLS_UTC_211_002 ...	Passed
Running test EDLS_UTC_211_003 ...	Passed
Running test EDLS_UTC_211_004 ...	Passed
Running test EDLS_UTC_211_005 ...	Passed
Running test EDLS_UTC_211_006 ...	Passed
Running test EDLS_UTC_211_007 ...	Passed
Running test EDLS_UTC_211_008 ...	Passed
Running test EDLS_UTC_211_009 ...	Passed
Running test EDLS_UTC_211_010 ...	Passed
Running test EDLS_UTC_211_011 ...	Passed
Running test EDLS_UTC_211_012 ...	Passed
Running test EDLS_UTC_211_013 ...	Passed
Running test EDLS_UTC_211_014 ...	Passed
Running test EDLS_UTC_211_015 ...	Passed
Running test EDLS_UTC_211_016 ...	Passed
Running test EDLS_UTC_211_017 ...	Passed
Running test EDLS_UTC_211_018 ...	Passed
Running test EDLS_UTC_211_019 ...	Passed
Running test EDLS_UTC_211_020 ...	Passed
Running test EDLS_UTC_211_021 ...	Passed
Running test EDLS_UTC_211_022 ...	Passed
Running test EDLS_UTC_211_023 ...	Passed
Running test EDLS_UTC_211_024 ...	Passed
Running test EDLS_UTC_211_025 ...	Passed
Running test EDLS_UTC_211_026 ...	Passed
Running test EDLS_UTC_211_027 ...	Passed
Running test EDLS_UTC_211_028 ...	Passed
Running test EDLS_UTC_211_029 ...	Passed
Running test EDLS_UTC_211_030 ...	Passed
Running test EDLS_UTC_211_031 ...	Passed
Running test EDLS_UTC_211_032 ...	Passed
Running test EDLS_UTC_212_000 ...	Passed
Running test EDLS_UTC_213_000 ...	Passed
Running test EDLS_UTC_214_000 ...	Passed
Running test EDLS_UTC_215_000 ...	Passed

PART 4 FINAL RESULT

LOCK CONTROLLER

Running Suite 2.1.6 Lock_Controller

Running test EDLS_UTC_216_000 ...	Passed
Running test EDLS_UTC_216_001 ...	Passed
Running test EDLS_UTC_216_002 ...	Passed
Running test EDLS_UTC_216_003 ...	Passed
Running test EDLS_UTC_216_004 ...	Passed
Running test EDLS_UTC_216_005 ...	Passed
Running test EDLS_UTC_216_006 ...	Passed
Running test EDLS_UTC_216_007 ...	Passed
Running test EDLS_UTC_216_008 ...	Passed
Running test EDLS_UTC_216_009 ...	Passed
Running test EDLS_UTC_216_010 ...	Passed
Running test EDLS_UTC_216_011 ...	Passed
Running test EDLS_UTC_216_012 ...	Passed
Running test EDLS_UTC_216_013 ...	Passed
Running test EDLS_UTC_216_014 ...	Passed
Running test EDLS_UTC_216_015 ...	Passed
Running test EDLS_UTC_216_016 ...	Passed
Running test EDLS_UTC_217_000 ...	Passed
Running test EDLS_UTC_218_000 ...	Passed

PART 4 FINAL RESULT

SOUND CONTROLLER

Running Suite 2.2.1 Sound_Controller	
Running test EDLS_UTC_221_000 ...	Passed
Running test EDLS_UTC_221_001 ...	Passed
Running test EDLS_UTC_221_002 ...	Passed
Running test EDLS_UTC_221_003 ...	Passed
Running test EDLS_UTC_221_004 ...	Passed
Running test EDLS_UTC_221_005 ...	Passed
Running test EDLS_UTC_221_006 ...	Passed
Running test EDLS_UTC_221_007 ...	Passed
Running test EDLS_UTC_221_008 ...	Passed
Running test EDLS_UTC_221_009 ...	Passed
Running test EDLS_UTC_221_010 ...	Passed
Running test EDLS_UTC_221_011 ...	Passed
Running test EDLS_UTC_221_012 ...	Passed
Running test EDLS_UTC_221_013 ...	Passed
Running test EDLS_UTC_221_014 ...	Passed
Running test EDLS_UTC_223_000 ...	Passed
Running test EDLS_UTC_224_000 ...	Passed
Running test EDLS_UTC_225_000 ...	Passed

PART 4 FINAL RESULT

LIGHT CONTROLLER & RESULT

Running Suite 2.2.2 Light_Controller

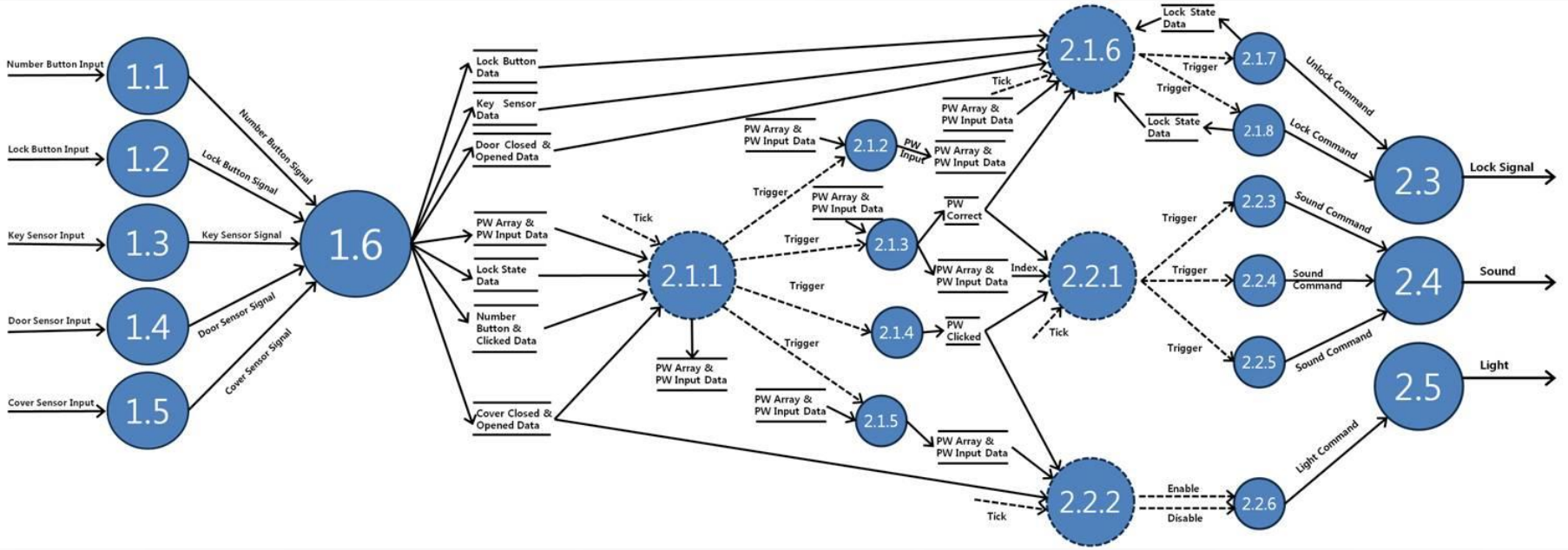
Running test EDLS_UTC_222_000 ...	Passed
Running test EDLS_UTC_222_001 ...	Passed
Running test EDLS_UTC_222_002 ...	Passed
Running test EDLS_UTC_222_003 ...	Passed
Running test EDLS_UTC_222_004 ...	Passed
Running test EDLS_UTC_222_005 ...	Passed
Running test EDLS_UTC_222_006 ...	Passed
Running test EDLS_UTC_222_007 ...	Passed
Running test EDLS_UTC_222_008 ...	Passed
Running test EDLS_UTC_222_009 ...	Passed
Running test EDLS_UTC_222_010 ...	Passed
Running test EDLS_UTC_222_011 ...	Passed
Running test EDLS_UTC_222_012 ...	Passed
Running test EDLS_UTC_222_013 ...	Passed
Running test EDLS_UTC_222_014 ...	Passed
Running test EDLS_UTC_226_000 ...	Passed

Cumulative Summary for Run				
Type	**Total**	**Run**	**Succeeded**	**Failed**
Suites	5	5	- NA -	0
Test Cases	109	109	109	0
Assertions	184	184	184	0

PART 5
SUMMARY

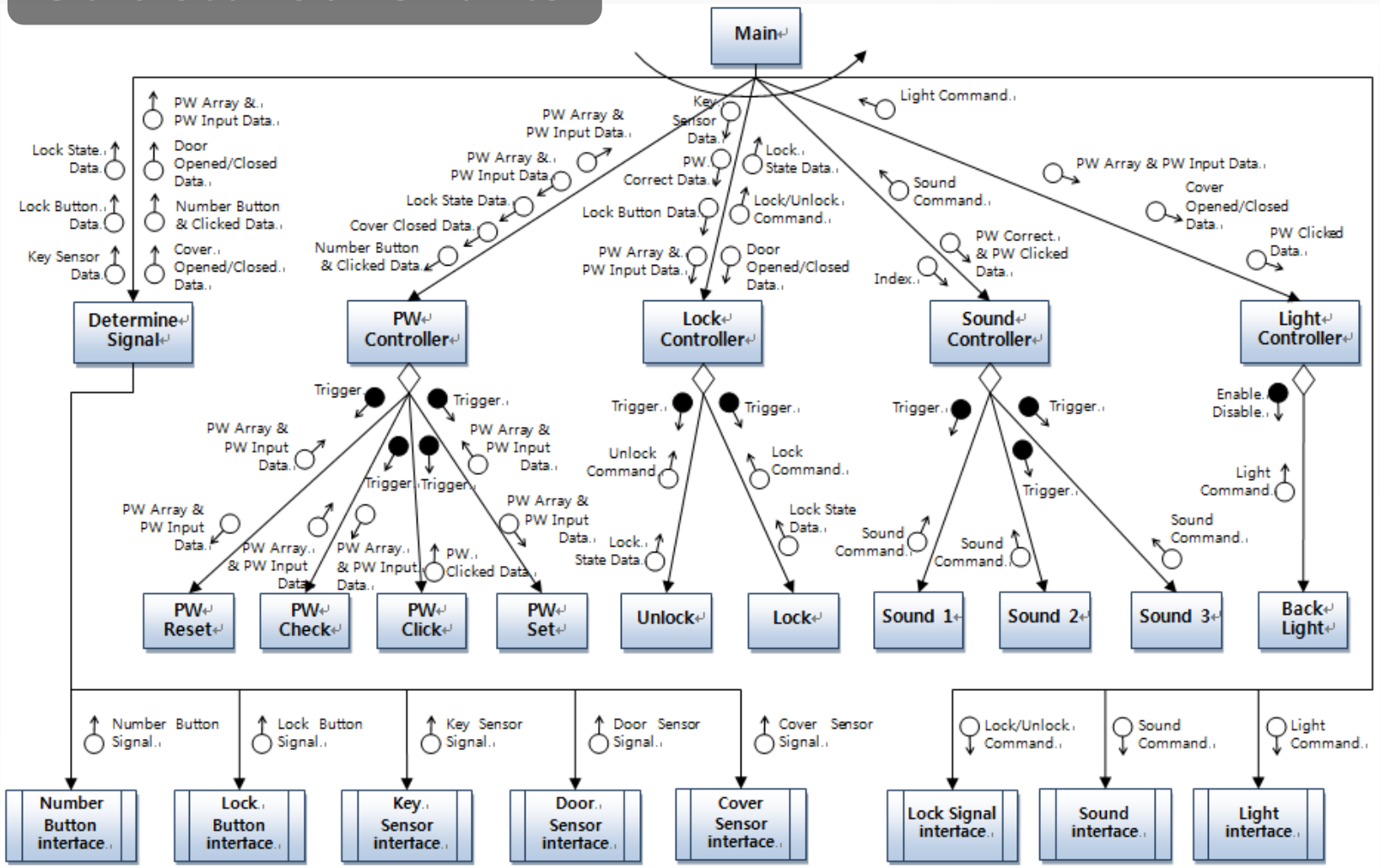
PART 5 SUMMARY

OVERALL DFD



PART 5 SUMMARY

Structured Charts



PART 5 SUMMARY

Demo

THANK YOU
ANY QUESTIONS?

기말고사 화이팅 !! ☺