gNuSMV(GetOut)

DMS Lab

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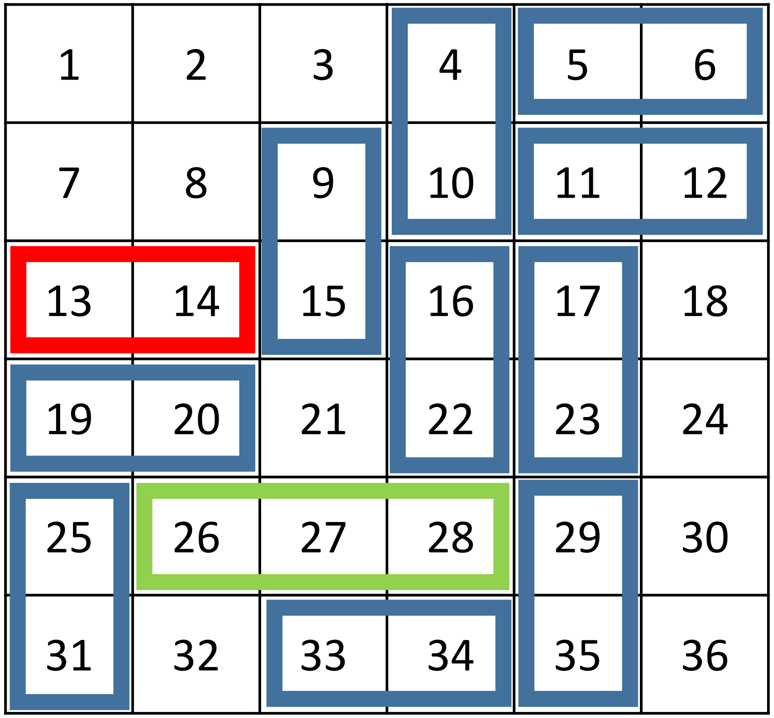
Oh Jun

Tiles

1	2	3	4	5	6
7	8	9	10	11	12
13	14	15	16	17	18
19	20	21	22	23	24
25	26	27	28	29	30
31	32	33	34	35	36

Blocks



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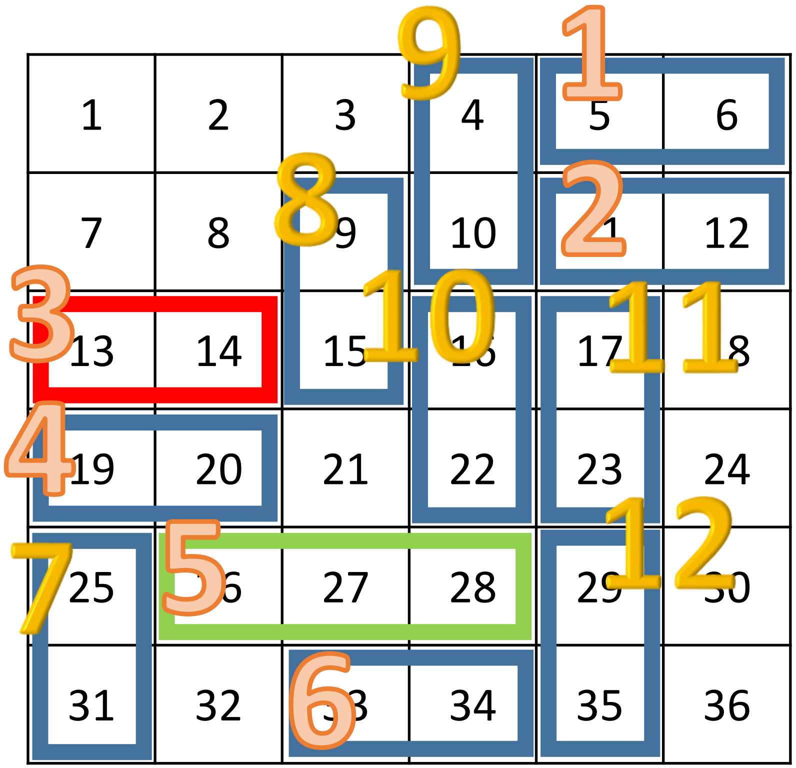
Block numbering



1	2	3	4	5	6
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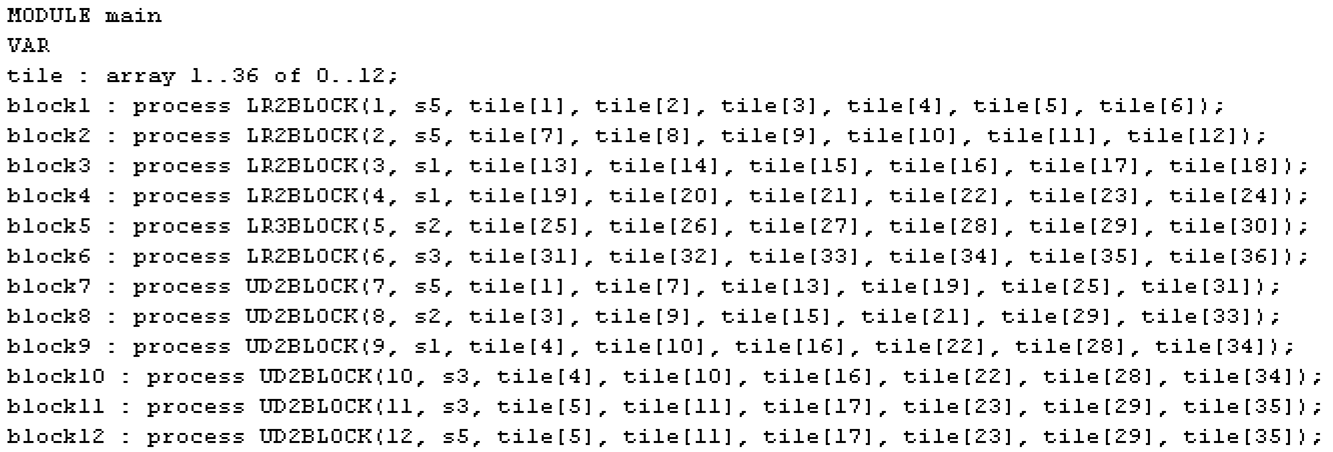
MODULE main

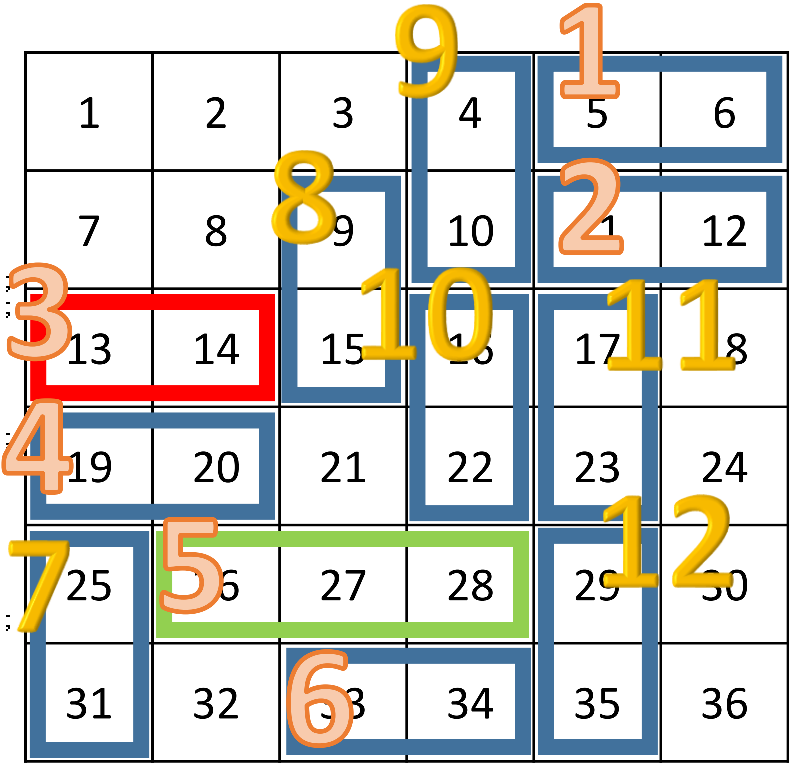


```
MODULE main
VAR
tile : array 1..36 of 0..12;
block1 : process LR2BLOCK(1, s5, tile[1], tile[2], tile[3], tile[4], tile[5], tile[6]);
block2 : process LR2BLOCK(2, s5, tile[7], tile[8], tile[9], tile[10], tile[11], tile[12]);
block3 : process LR2BLOCK(3, s1, tile[13], tile[14], tile[15], tile[16], tile[17], tile[18]);
block4 : process LR2BLOCK(4, s1, tile[19], tile[20], tile[21], tile[22], tile[23], tile[24]);
block5 : process LR3BLOCK(5, s2, tile[25], tile[26], tile[27], tile[28], tile[29], tile[30]);
block6 : process LR2BLOCK(6, s3, tile[31], tile[32], tile[33], tile[34], tile[35], tile[36]);
block7 : process UD2BLOCK(7, s5, tile[1], tile[7], tile[13], tile[19], tile[25], tile[31]);
block8 : process UD2BLOCK(8, s2, tile[3], tile[9], tile[15], tile[21], tile[29], tile[33]);
block9 : process UD2BLOCK(9, s1, tile[4], tile[10], tile[16], tile[22], tile[28], tile[34]);
block10 : process UD2BLOCK(10, s3, tile[4], tile[10], tile[16], tile[22], tile[28], tile[34]);
block11 : process UD2BLOCK(11, s3, tile[5], tile[11], tile[17], tile[23], tile[29], tile[35]);
block12 : process UD2BLOCK(12, s5, tile[5], tile[11], tile[17], tile[23], tile[29], tile[35]);
```

MODULE main

0	0	0	9	1	1
0	0	8	9	2	2
3	3	8	10	11	0
4	4	0	10	11	0
7	5	5	5	12	0
7	0	6	6	12	0

```
ASSIGN
init(tile[1]) := 0;
init(tile[2]) := 0;
init(tile[3]) := 0;
init(tile[4]) := 9;
init(tile[5]) := 1;
init(tile[6]) := 1;
init(tile[7]) := 0;
init(tile[8]) := 0;
init(tile[9]) := 8;
init(tile[10]) := 9;
init(tile[11]) := 2;
init(tile[12]) := 2;
init(tile[13]) := 3;
init(tile[14]) := 3;
init(tile[15]) := 8;
init(tile[16]) := 10;
init(tile[17]) := 11;
init(tile[18]) := 0;
init(tile[19]) := 4;
init(tile[20]) := 4;
init(tile[21]) := 0;
init(tile[22]) := 10;
init(tile[23]) := 11;
init(tile[24]) := 0;
init(tile[25]) := 7;
init(tile[26]) := 5;
init(tile[27]) := 5;
init(tile[28]) := 5;
init(tile[29]) := 12;
init(tile[30]) := 0;
init(tile[31]) := 7;
init(tile[32]) := 0;
init(tile[33]) := 6;
init(tile[34]) := 6;
init(tile[35]) := 12;
init(tile[36]) := 0;
```



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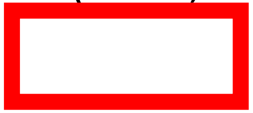
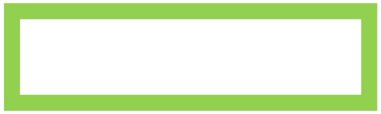
MODULE block

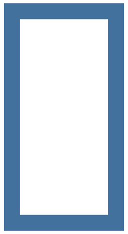
- LR2BLOCK
  - MODULE LR2BLOCK(index, initstate, tile1, tile2, tile3, tile4, tile5, tile6)



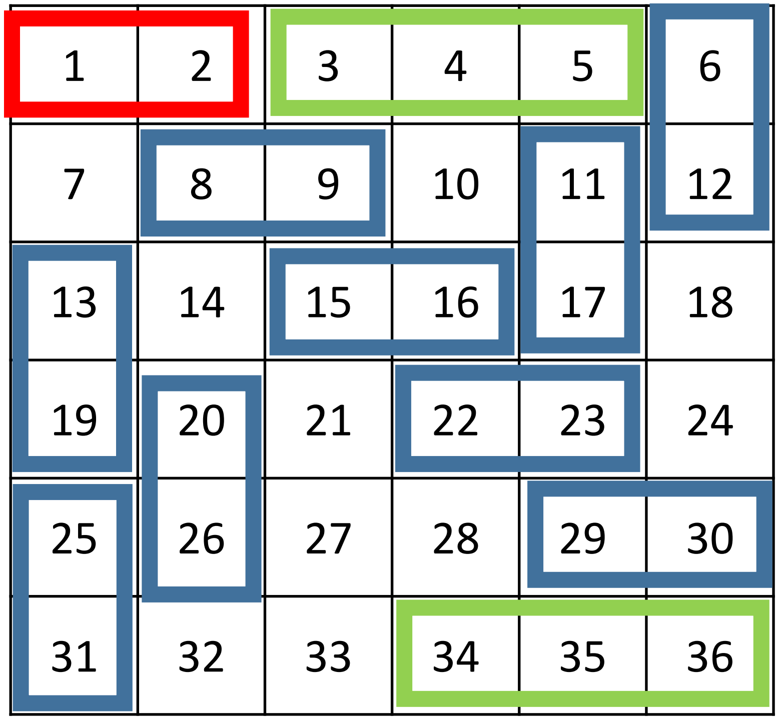
- LR3BLOCK
  - MODULE LR3BLOCK(index, initstate, tile1, tile2, tile3, tile4, tile5, tile6)



- UD2BLOCK
  - MODULE LR3BLOCK(index, initstate, tile1, tile2, tile3, tile4, tile5, tile6)



BLOCK state



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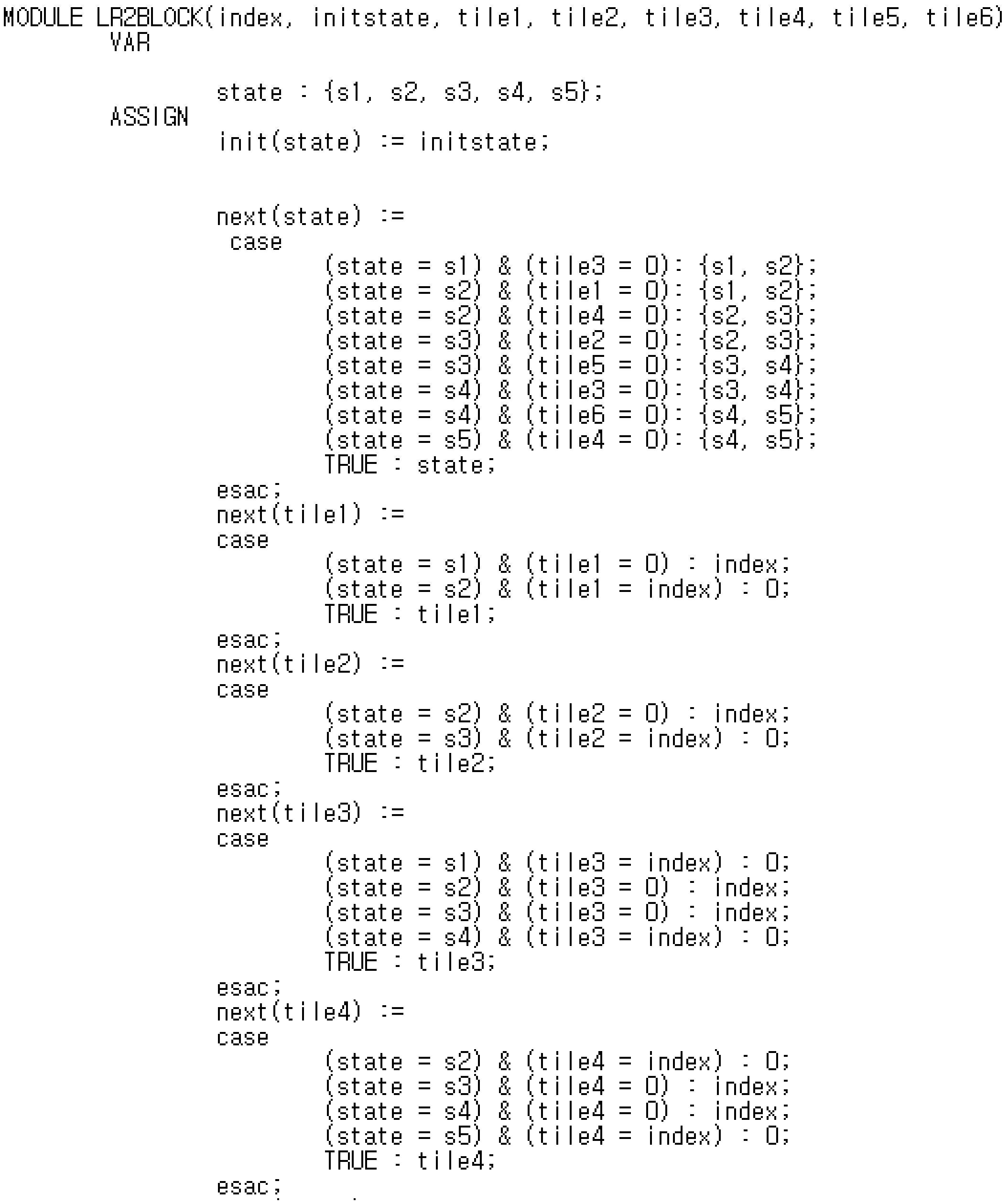
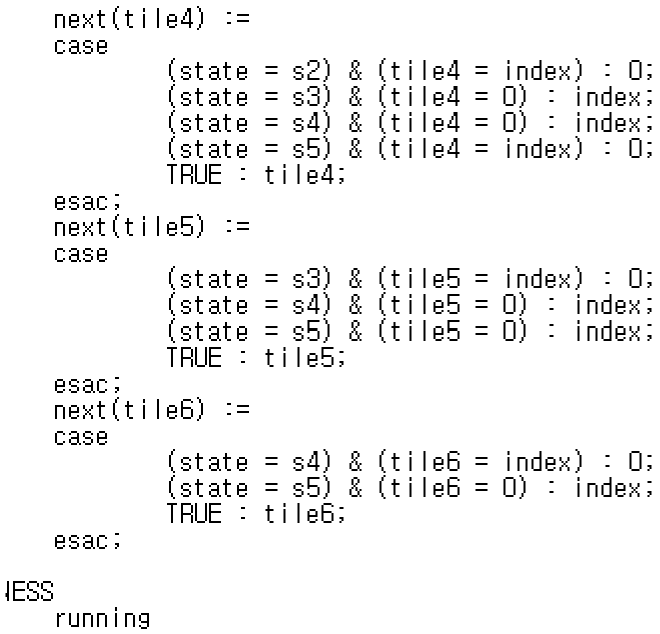
31	32	33	34	35	36

```
MODULE LR2BLOCK(index, initstate, tile1, tile2, tile3, tile4, tile5, tile6)
        VAR

                state : {s1, s2, s3, s4, s5};


MODULE LR3BLOCK(index, initstate, tile1, tile2, tile3, tile4, tile5, tile6)
        VAR

                state : {s1, s2, s3, s4};

MODULE UD2BLOCK(index, initstate, tile1, tile2, tile3, tile4, tile5, tile6)
        VAR

                state : {s1, s2, s3, s4, s5};
```

Model code

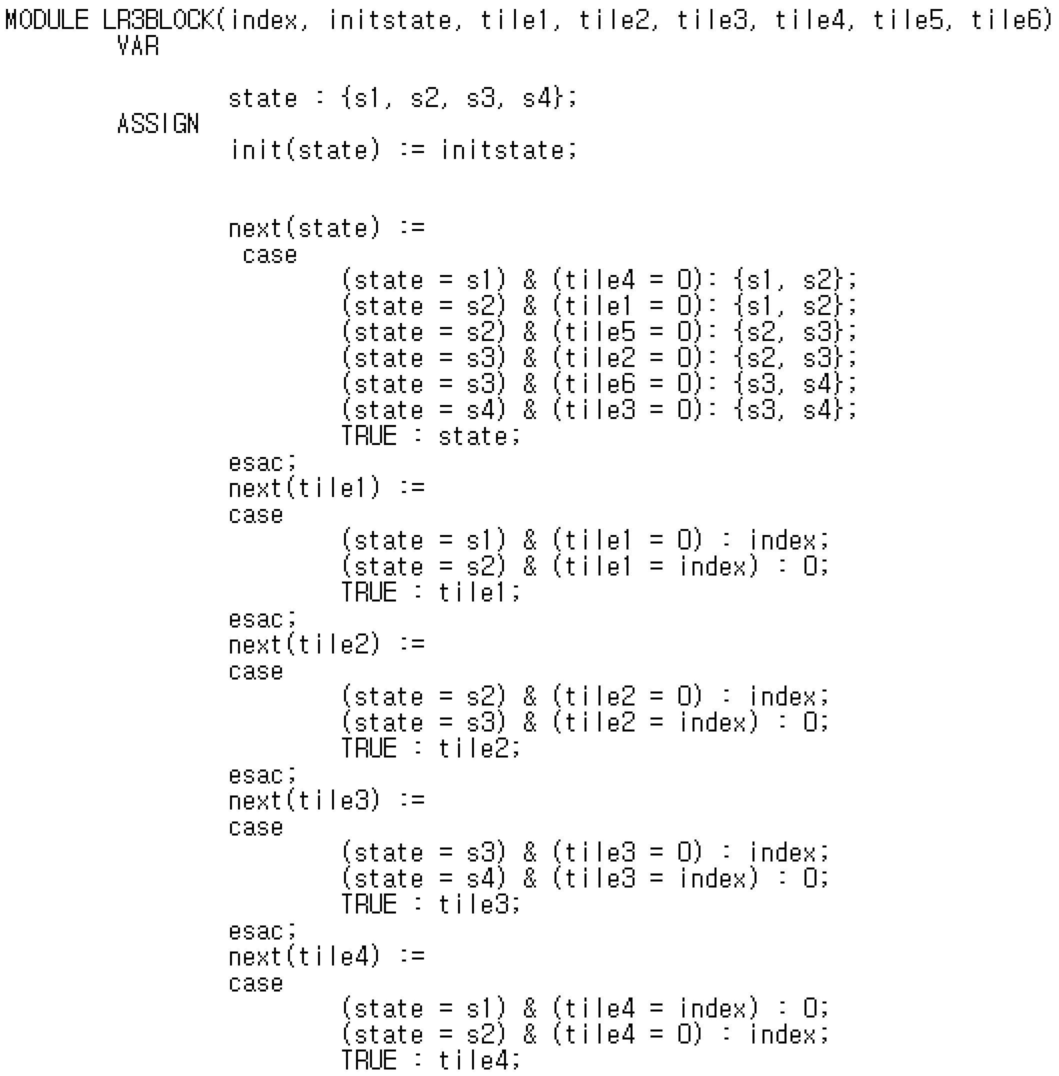


```
MODULE LR2BLOCK(index, initstate, tile1, tile2, tile3, tile4, tile5, tile6)
        VAR

                state : {s1, s2, s3, s4, s5};
        ASSIGN
                init(state) := initstate;


                next(state) :=
                 case
                        (state = s1) & (tile3 = 0): {s1, s2};
                        (state = s2) & (tile1 = 0): {s1, s2};
                        (state = s2) & (tile4 = 0): {s2, s3};
                        (state = s3) & (tile2 = 0): {s2, s3};
                        (state = s3) & (tile5 = 0): {s3, s4};
                        (state = s4) & (tile3 = 0): {s3, s4};
                        (state = s4) & (tile6 = 0): {s4, s5};
                        (state = s5) & (tile4 = 0): {s4, s5};
                        TRUE : state;
                esac;
                next(tile1) :=
                case
                        (state = s1) & (tile1 = 0) : index;
                        (state = s2) & (tile1 = index) : 0;
                        TRUE : tile1;
                esac;
                next(tile2) :=
                case
                        (state = s2) & (tile2 = 0) : index;
                        (state = s3) & (tile2 = index) : 0;
                        TRUE : tile2;
                esac;
                next(tile3) :=
                case
                        (state = s1) & (tile3 = index) : 0;
                        (state = s2) & (tile3 = 0) : index;
                        (state = s3) & (tile3 = 0) : index;
                        (state = s4) & (tile3 = index) : 0;
                        TRUE : tile3;
                esac;
                next(tile4) :=
                case
                        (state = s2) & (tile4 = index) : 0;
                        (state = s3) & (tile4 = 0) : index;
                        (state = s4) & (tile4 = 0) : index;
                        (state = s5) & (tile4 = index) : 0;
                        TRUE : tile4;
                esac;
```

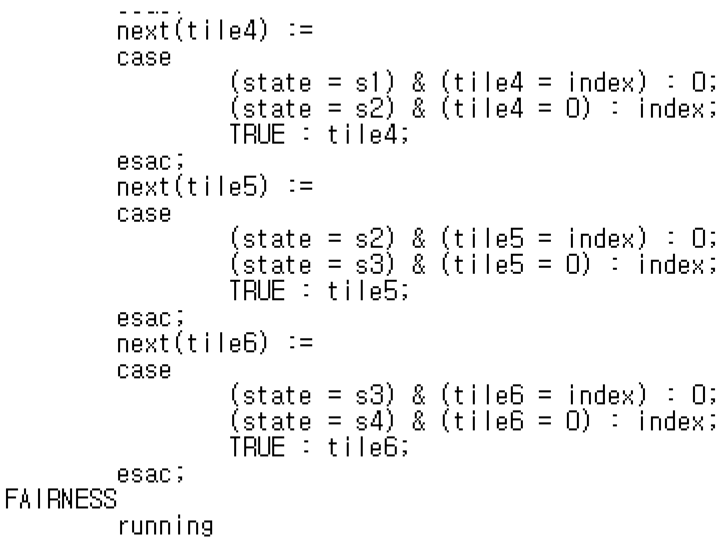


```
    next(tile4) :=
    case
            (state = s2) & (tile4 = index) : 0;
            (state = s3) & (tile4 = 0) : index;
            (state = s4) & (tile4 = 0) : index;
            (state = s5) & (tile4 = index) : 0;
            TRUE : tile4;
    esac;
    next(tile5) :=
    case
            (state = s3) & (tile5 = index) : 0;
            (state = s4) & (tile5 = 0) : index;
            (state = s5) & (tile5 = 0) : index;
            TRUE : tile5;
    esac;
    next(tile6) :=
    case
            (state = s4) & (tile6 = index) : 0;
            (state = s5) & (tile6 = 0) : index;
            TRUE : tile6;
    esac;

IESS
    running
```

Model code

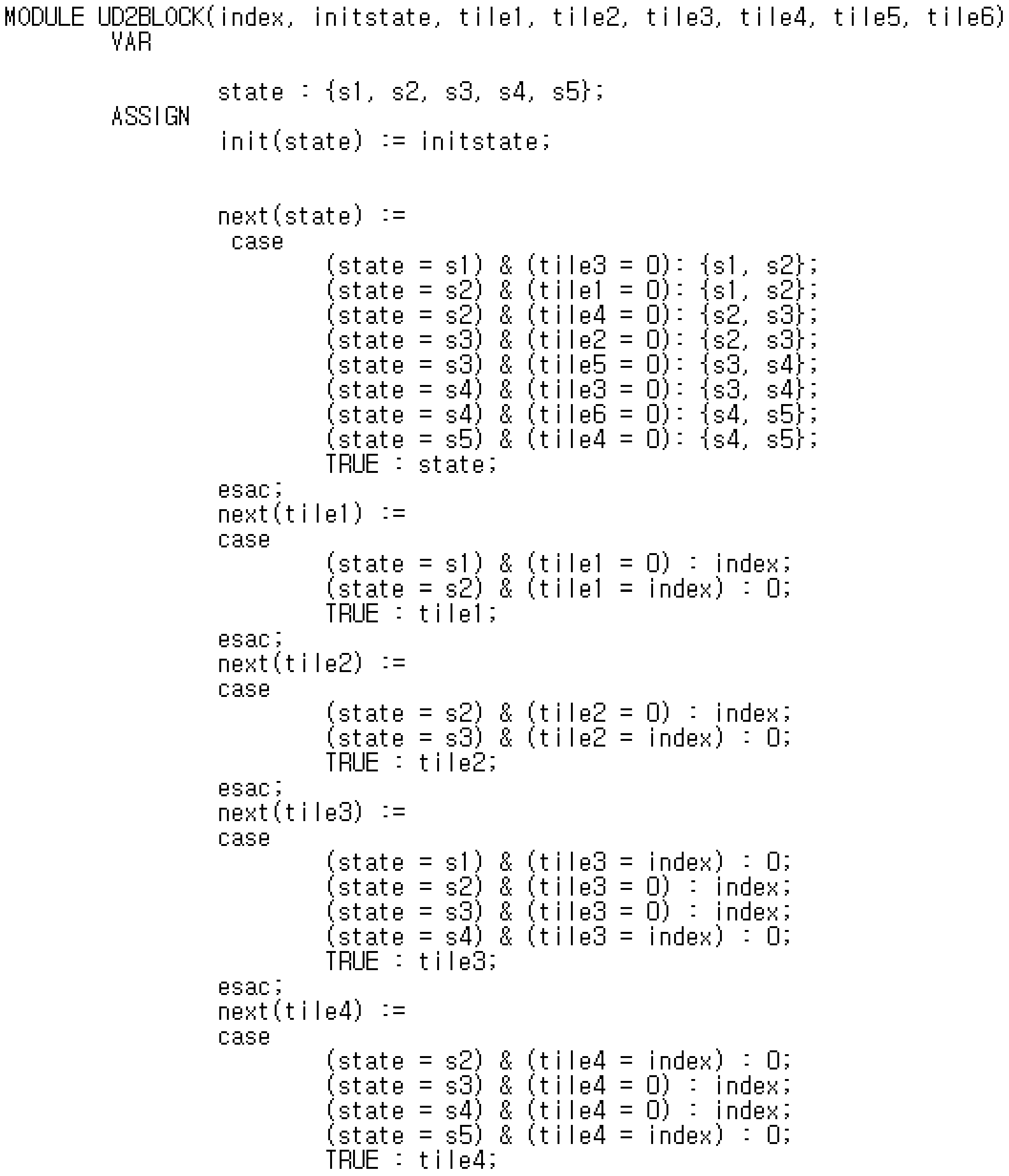


```
MODULE LR3BLOCK(index, initstate, tile1, tile2, tile3, tile4, tile5, tile6)
        VAR

                state : {s1, s2, s3, s4};
        ASSIGN
                init(state) := initstate;


                next(state) :=
                 case
                        (state = s1) & (tile4 = 0): {s1, s2};
                        (state = s2) & (tile1 = 0): {s1, s2};
                        (state = s2) & (tile5 = 0): {s2, s3};
                        (state = s3) & (tile2 = 0): {s2, s3};
                        (state = s3) & (tile6 = 0): {s3, s4};
                        (state = s4) & (tile3 = 0): {s3, s4};
                        TRUE : state;
                esac;
                next(tile1) :=
                case
                        (state = s1) & (tile1 = 0) : index;
                        (state = s2) & (tile1 = index) : 0;
                        TRUE : tile1;
                esac;
                next(tile2) :=
                case
                        (state = s2) & (tile2 = 0) : index;
                        (state = s3) & (tile2 = index) : 0;
                        TRUE : tile2;
                esac;
                next(tile3) :=
                case
                        (state = s3) & (tile3 = 0) : index;
                        (state = s4) & (tile3 = index) : 0;
                        TRUE : tile3;
                esac;
                next(tile4) :=
                case
                        (state = s1) & (tile4 = index) : 0;
                        (state = s2) & (tile4 = 0) : index;
                        TRUE : tile4;
```

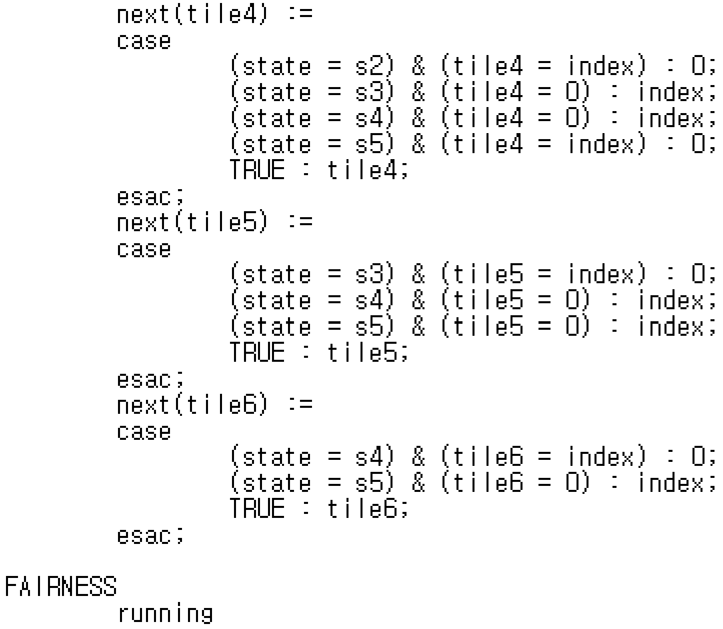


```
        next(tile4) :=
        case
                (state = s1) & (tile4 = index) : 0;
                (state = s2) & (tile4 = 0) : index;
                TRUE : tile4;
        esac;
        next(tile5) :=
        case
                (state = s2) & (tile5 = index) : 0;
                (state = s3) & (tile5 = 0) : index;
                TRUE : tile5;
        esac;
        next(tile6) :=
        case
                (state = s3) & (tile6 = index) : 0;
                (state = s4) & (tile6 = 0) : index;
                TRUE : tile6;
        esac;
FAIRNESS
        running
```

Model code



```
MODULE UD2BLOCK(index, initstate, tile1, tile2, tile3, tile4, tile5, tile6)
        VAR
                state : {s1, s2, s3, s4, s5};
        ASSIGN
                init(state) := initstate;

                next(state) :=
                 case
                        (state = s1) & (tile3 = 0): {s1, s2};
                        (state = s2) & (tile1 = 0): {s1, s2};
                        (state = s2) & (tile4 = 0): {s2, s3};
                        (state = s3) & (tile2 = 0): {s2, s3};
                        (state = s3) & (tile5 = 0): {s3, s4};
                        (state = s4) & (tile3 = 0): {s3, s4};
                        (state = s4) & (tile6 = 0): {s4, s5};
                        (state = s5) & (tile4 = 0): {s4, s5};
                        TRUE : state;
                esac;
                next(tile1) :=
                case
                        (state = s1) & (tile1 = 0) : index;
                        (state = s2) & (tile1 = index) : 0;
                        TRUE : tile1;
                esac;
                next(tile2) :=
                case
                        (state = s2) & (tile2 = 0) : index;
                        (state = s3) & (tile2 = index) : 0;
                        TRUE : tile2;
                esac;
                next(tile3) :=
                case
                        (state = s1) & (tile3 = index) : 0;
                        (state = s2) & (tile3 = 0) : index;
                        (state = s3) & (tile3 = 0) : index;
                        (state = s4) & (tile3 = index) : 0;
                        TRUE : tile3;
                esac;
                next(tile4) :=
                case
                        (state = s2) & (tile4 = index) : 0;
                        (state = s3) & (tile4 = 0) : index;
                        (state = s4) & (tile4 = 0) : index;
                        (state = s5) & (tile4 = index) : 0;
                        TRUE : tile4;
```



```
                next(tile4) :=
                case
                        (state = s2) & (tile4 = index) : 0;
                        (state = s3) & (tile4 = 0) : index;
                        (state = s4) & (tile4 = 0) : index;
                        (state = s5) & (tile4 = index) : 0;
                        TRUE : tile4;
                esac;
                next(tile5) :=
                case
                        (state = s3) & (tile5 = index) : 0;
                        (state = s4) & (tile5 = 0) : index;
                        (state = s5) & (tile5 = 0) : index;
                        TRUE : tile5;
                esac;
                next(tile6) :=
                case
                        (state = s4) & (tile6 = index) : 0;
                        (state = s5) & (tile6 = 0) : index;
                        TRUE : tile6;
                esac;

        FAIRNESS
                running
```

Property

- EF(block3.state = s5)

Problems

- 모델이 잘못 된건가…
- 프로퍼티가 잘못 된건가…
- 상태 폭발이라 불가능한 건가…

Thank You